REMARKS

Claims 1-20 are pending. Claims 1-20 are rejected. The Applicants respectfully request further examination and reconsideration in view of the following remarks.

112 Rejection

Claims 1-20 are rejected under 35 USC 112, second paragraph as being indefinite. The Examiner contends that the Claims 1, 10 and 19 limitation, namely, "that enable the processor units themselves" is not understood because "the correspondence among the processor units of the 'cache coherent snooping commands' and the instant processor units is not clear." The Applicants respectfully submit that the aforementioned limitation should be interpreted to convey its plain uncomplicated meaning, which is that the recited processors themselves are enabled to ensure cache coherency through snooping. As this limitation particularly points out and distinctly claims the subject matter of the invention and is indeed definite, the Applicants respectfully request the withdrawal of the 35 USC 112 rejection of Claims 1-20.

102 Rejection

Claims 1-4, 7 and 9 are rejected under 35 U.S.C. § 102(e) as being anticipated by Arimilli et al. (U.S. Patent No. 6,587,926). The Applicants have reviewed the cited reference and respectfully submit that the embodiments of the present invention as are recited in Claims 1-4, 7 and 9 are neither anticipated nor rendered obvious by Arimilli et al.

The Examiner is respectfully directed to independent Claim 1. Claim 1 is drawn to a cache coherent multiple processor integrated circuit that comprises:

> ...an embedded RAM unit for storing instructions and data for the processor units; a cache coherent bus

coupled to the processor units and the embedded RAM unit, the bus configured to provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit.

Claims 2-4, 7 and 9 depend from Claim 1 and recite additional limitations of the claimed invention.

Arimilli et al. does not anticipate or render obvious a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 1. It should be appreciated that the Arimilli et al. reference is concerned with the management of data access transactions within a data storage system and not with providing cache coherency between cache units for a processor and an embedded RAM unit as claimed.

In contrast to the invention embodiments set forth in Applicants' claims, in the system that is disclosed by Arimilli et al. snooping is performed by storage devices (or internal processors thereof) and third party transactors (see column 9, lines 35-40). Importantly, in the system that is disclosed by Arimilli et al. there is no teaching or suggestion that the snooping is for ensuring cache coherency between cache units for processors and an embedded RAM unit as is recited in Claim 1. Moreover, Arimilli et al. teaches sharply away from these claimed features of the invention embodiments as Arimilli et al. shows in Figure 5 that in his disclosed system a snoop request is made when a coherency update is not needed (see step 510).

Indeed, nowhere in the Arimilli et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in claim 1. Consequently, Arimilli et al. does not anticipate or render obvious the embodiment of the Applicants' invention set forth in Claim 1.

The Examiner is reminded that in order to anticipate a claim a reference must teach each and every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed Cir. 1987). It is clear from the discussion above that "each and every element" of Claim 1 is in fact not described by the Arimilli et al. reference. More specifically, Arimilli et al. does not "either expressly or inherently" show or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 1.

Accordingly, Applicants respectfully submit that Arimilli et al. does not anticipate or render obvious the embodiments of the Applicants' invention as are recited in Claims 2-4, 7 and 9 as these Claims are dependent on Claim 1. Therefore, these Claims overcome the rejection under 35 U.S.C. 102(e) as being dependent on allowable Claim 1.

103 Rejection

Claim 5 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Arimilli et al. (U.S. Patent No. 6,571,322). Arimilli et al. (U.S. Patent No. 6,571,322) does not teach or suggest a modification of Arimilli et al. (U.S. Patent No. 6,587,926) that will remedy the deficiencies of Arimilli et al. (U.S. Patent No. 6,587,926) outlined above. More specifically, Arimilli et al. (U.S. Patent No. 6,571,322) does not teach or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 1 (from which Claim 5 depends).

Arimilli et al. (U.S. Patent No. 6,571,322) only shows a multiprocessor computer system with a mechanism for cache intervention. Nowhere in the Arimilli et al. (U.S. Patent No. 6,571,322) reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in claim 1 (from which Claim 5 depends). Consequently, Arimilli et al. (U.S. Patent No. 6,587,926) either alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious the embodiment of Applicants' invention as set forth in Claim 1 (from which Claim 5 depends). Accordingly, Applicants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claim 5 dependent on Claim 1 and that Claim 5 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Miller et al. (U.S. Patent No. 6,560,682). Miller et al. does not teach or suggest a modification of Arimilli et al. that remedies the deficiencies of Arimilli et al outlined above. More specifically, Miller et al. does not teach or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 1 (from which Claim 6 depends).

Miller et al. only shows a system and method for terminating lock-step sequences in multiprocessor systems. Nowhere in the Miller et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in Claim 1 (from which Claim 6 depends). Consequently, Arimilli et al. either alone or in combination with Miller et al. does not anticipate or render obvious the embodiment of the Applicants' invention as set forth in Claim 1 (from which Claim 6 depends). Accordingly, Applicants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Miller et al. (U.S. Patent No. 6,560,682) does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claim 6 dependent on Claim 1 and that Claim 6 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Bitar et al. (U.S. Patent No. 6,418,460). Bitar et al. does not teach or suggest a modification of Arimilli et al. that remedies the deficiencies of Arimilli et al. outlined above. More specifically, Bitar et al. does not teach or suggest a cache

coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 1 (from which Claim 8 depends).

Bitar et al. only shows a system and method for finding preempted threads in a multi-threaded application. Nowhere in the Bitar et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in Claim 1 (from which Claim 8 depends). Consequently, Arimilli et al. either alone or in combination with Bitar et al., does not anticipate or render obvious the embodiment of the Applicants' invention as set forth in Claim 1 (from which Claim 8 depends). Accordingly, Applicants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Bitar et al. (U.S. Patent No. 6,418,460) does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claim 8 dependent on Claim 1 and that Claim 8 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Claims 10-13, 16 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Sherburne (U.S. Patent Application Publication No. 2002/0184546). Sherburne does not teach or suggest a modification of Arimilli et al. that remedies the deficiencies of Arimilli et al. outlined above. More specifically, Sherburne does not teach or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as

is recited in Claim 10. Sherburne only shows a method and device for modifying the contents of memory.

Nowhere in the Sherburne et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in claim 10. Consequently, Arimilli et al. either alone or in combination with Sherburne does not anticipate or render obvious the embodiment of the Applicants' invention as set forth in Claim 10. Accordingly, Applicants respectfully submit that Arimilli et al. alone or in combination with Sherburne does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claims 11-13, 16 and 18 dependent on Claim 10 and that these Claims overcome the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Claim 14 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Arimilli et al. (U.S. Patent No. 6,571,322). Arimilli et al. (U.S. Patent No. 6,571,322) does not teach or suggest a modification of Arimilli et al. (U.S. Patent No. 6,587,926) that remedies the deficiencies of Arimilli et al. (U.S. Patent No. 6,587,926) outlined above. More specifically, Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 10 (from which Claim 14 depends). Arimilli et al. (U.S. Patent No. 6,571,322) only shows a multiprocessor computer system with a mechanism for cache intervention.

Nowhere in the Arimilli et al. (U.S. Patent No. 6,571,322) reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in Claim 10 (from which Claim 14 depends). Consequently, Arimilli et al. (U.S. Patent No. 6,587,926) either alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious the embodiment of the Applicants' invention as set forth in Claim 10 (from which Claim 14 depends). Accordingly, Applicants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claim 14 dependent on Claim 10 and that Claim 14 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Miller et al. (U.S. Patent No. 6,560,682). Miller et al. does not teach or suggest a modification of Arimilli et al. that remedies the deficiencies of Arimilli et al. outlined above. More specifically, Miller et al. does not teach or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 10 (from which Claim 15 depends). Miller et al. only shows a system and method for terminating lock-step sequences in multiprocessor systems.

Nowhere in the Miller et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in Claim 10 (from which Claim 15 depends). Consequently, Arimilli et al. either alone or in combination with Miller et al. does not anticipate or render obvious the embodiment of the Applicants' invention as set forth in Claim 10 (from which Claim 15 depends). Accordingly, Applicants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Miller et al. (U.S. Patent No. 6,560,682) does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claim 15 dependent on Claim 10 and that Claim 15 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Claim 17 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Miller et al. (U.S. Patent No. 6,560,682). Miller et al. does not teach or suggest a modification of Arimilli et al. that remedies the deficiencies of Arimilli et al. outlined above. More specifically, Miller et al. does not teach or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 10 (from which Claim 17 depends). Miller et al. only shows a system and method for terminating lock-step sequences in multiprocessor systems.

Nowhere in the Miller et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves

to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in Claim 10 (from which Claim 17 depends). Consequently, Arimilli et al. either alone or in combination with Miller et al. does not anticipate or render obvious the embodiment of the Applicants' invention as set forth in Claim 10 (from which Claim 17 depends). Accordingly, Applicants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Miller et al. (U.S. Patent No. 6,560,682) does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claim 17 dependent on Claim 10 and that Claim 17 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Claims 19 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Sherburne (U.S. Patent Application Publication No. 2002/0184546) and further in view of Arimilli et al. (U.S. Patent No. 6,571,322). Arimilli et al. (U.S. Patent No. 6,571,322) does not teach or suggest a modification of Arimilli et al. (U.S. Patent No. 6,587,926) and Sherburne (U.S. Patent Application Publication No. 2002/0184546) that remedies the deficiencies of Arimilli et al. outlined above. More specifically, Arimilli et al. (U.S. Patent No. 6,571,322) does not teach or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 19. Arimilli et al. (U.S. Patent No. 6,571,322) only shows a multiprocessor computer system with a mechanism for cache intervention.

Nowhere in the Arimilli et al. (U.S. Patent No. 6,571,322) reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in claim 19. Consequently, Arimilli et al. (U.S. Patent No. 6,587,926) either alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) and Sherburne (U.S. Patent Application Publication No. 2002/0184546) does not anticipate or render obvious the embodiment of the Applicants invention as set forth in Claim 19. Accordingly, Applicants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claim 20 dependent on Claim 19 and that Claim 20 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Conclusion

In light of the above-listed amendments and remarks, Applicants respectfully request allowance of the remaining Claims.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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